AMENDMENT TO THE CLAIMS

Claims 1-11 (Cancelled)

Claim 12 (Currently Amended): An electrostatic discharge (ESD) protection circuit, comprising:

a silicon controlled switch (SCS) connected between a positive power supply node and a negative power supply node, where the SCS being formed by an NPN transistor and a PNP transistor,

wherein an anode of the SCS is formed by an emitter of the PNP transistor, a base of the PNP transistor is connected to the positive power supply node through a resistor R_N and is connected to a collector of the NPN transistor, a collector of the PNP transistor is connected to a base of the NPN transistor and further through a resister R_{sub} to a ground terminal, where the base of the PNP transistor serving as a gate of the SCS;

a switch control circuit connected between the positive power supply node and the gate of the SCS;

a metal oxide semiconductor field effect transistor (MOSFET) having a drain, a source and a ~~source~~ gate, ~~which~~ wherein the drain and the source of the MOSFET are respectively connected to the SCS and the ground terminal, and the gate of the MOSFET is ~~having a gate~~ coupled to a transistor control circuit, ~~to~~ wherein the MOSFET can cause the SCS to be triggered into a conduction status~~,~~; and

the transistor control circuit ~~being~~ is connected to the positive power supply node and the MOSFET;

~~such that~~ whereby when forward over-voltage stress occurs over the positive power

supply node, ~~enables~~ the transistor control circuit is enabled to turn on the MOSFET, and at the same time the switch control circuit is enabled to trigger the SCS into a conduction status to form a discharging path, such that ~~thereby to decrease~~ a terminal voltage over the positive power supply node is decreased to a level of a holding voltage of the SCS to provide an ESD protection and prevent latch-up of the SCS.

Claim 13 (Previously Added): The ESD protection circuit as claimed in claim 12, wherein the transistor control circuit is formed by a capacitor connected to a resistor in series at a node, the node is connected to the gate of the MOSFET, such that a time constant of the transistor control circuit is determined by adjusting values of the capacitor and the resistor to control a conduction time of the MOSFET.

Claim 14 (Previously Added): The ESD protection circuit as claimed in claim 12, wherein the switch control circuit has a Zener diode connected across the bases of the PNP transistor and the NPN transistor in the SCS, so that a discharge current can continue after the MOSFET is disabled.

Claim 15 (Previously Added): The ESD protection circuit as claimed in claim 14, wherein the Zener diode of the switch control circuit is further connected to a diode in series between the bases of the PNP transistor and the NPN transistor.

Claim 16 (Previously Added): The ESD protection circuit is claimed in claim 12, wherein the SCS is connected to the ground terminal through a diode array in series.

Claim 17 (Previously Added): The ESD protection circuit as claimed in claim 13, wherein the SCS is connected to the ground terminal through a diode array in series.

Claim 18 (Previously Added): The ESD protection circuit as claimed in claim 14, wherein the SCS is connected to the ground terminal through a diode array in series.

Claim 19 (Previously Added): The ESD protection circuit as claimed in claim 15, wherein the SCS is connected to the ground terminal through a diode array in series.

Claim 20 (Previously Added): The ESD protection circuit as claimed in claim 12, wherein the switch control has an NMOS transistor connected across the bases of the PNP transistor and the NPN transistor of the SCS.

Claim 21 (Currently Amended): An electrostatic discharge (ESD) protection circuit, comprising:

a silicon controlled switch (SCS) connected between a positive power supply node and a negative power supply node, the SCS ~~being~~ is formed by an NPN transistor and a PNP transistor,

wherein an anode of the SCS is formed by an emitter of the PNP transistor, a base of the PNP transistor is connected to a resistor ~~R_N~~ (R_N) and is connected to a collector of the NPN transistor, a collector of the PNP transistor is connected to a base of the NPN transistor and further through a resistor ~~R_{SUB}~~ (R_{SUB}) to a ground terminal, where the base of the PNP transistor ~~serving~~ serves as a gate of the SCS;

a switch control circuit connected between the negative power supply node and the gate of the SCS;

a metal oxide semiconductor field effect transistor (MOSFET) having a drain, ~~and~~ a source and a gate ~~which~~ wherein the drain and the source of the MOSFET are respectively connected to the positive power supply node and the SCS, and the ~~MOSFET having a~~ gate of the MOSFET is coupled to a transistor control circuit, wherein the MOSFET can ~~to~~ cause the SCS to be triggered into a conduction status~~,~~; and

the transistor control circuit ~~being~~ is connected to the positive power supply node and the MOSFET;

~~such that~~ whereby when forward over-voltage stress occurs over the positive power supply node, ~~enables~~ the transistor control circuit is enabled to turn on the MOSFET, and at the same time the switch control circuit is enabled to trigger the SCS into a conduction status to form a discharging path, ~~thereby to decrease a~~ such that a terminal voltage over the positive power supply node is decreased to a level of a holding voltage of the SCS to provide an ESD protection and prevent latch-up of the SCS.

Claim 22 (Previously Added): The ESD protection circuit as claimed in claim 21, wherein the transistor control circuit is formed by a capacitor connected to a resistor in series at a node, and the node is connected to the gate of the MOSFET, such that a time constant of the transistor control circuit is determined by adjusting values of the capacitor and the resistor to control a conduction time of the MOSFET.

Claim 23 (Previously Added): The ESD protection circuit as claimed in claim 21, wherein the switch control circuit has a Zener diode connected across the bases of the PNP transistor and the NPN transistor of the SCS, so that a discharge current can continue after the MOSFET is disabled.

Claim 24 (Previously Added): The ESD protection circuit as claimed in claim 23, wherein the Zener diode of the switch control circuit is further connected to a diode in series between the bases of the PNP transistor and the NPN transistor.

Claim 25 (Previously Added): The ESD protection circuit as claimed in claim 21, wherein the SCS is connected to the positive power supply node through a diode array in series.

Claim 26 (Previously Added): The ESD protection circuit as claimed in claim 22, wherein the SCS is connected to the positive power supply node through a diode array in series.

Claim 27 (Previously Added): The ESD protection circuit as claimed in claim 23,

wherein the SCS is connected to the positive power supply node through a diode array in series.

Claim 28 (Previously Added): The ESD protection circuit as claimed in claim 24, wherein the SCS is connected to the positive power supply node through a diode array in series.

Claim 29 (Currently Amended): An electrostatic discharge (ESD) protection circuit, comprising:

a silicon controlled switch (SCS) connected between a positive power supply node and a negative power supply node, where the SCS ~~being~~ is formed by an NPN transistor and a PNP transistor,

wherein a base of the PNP transistor is connected to the positive power supply node through a resistor ~~R_{SUB}~~ (R_{SUB}) and is connected to a collector of the NPN transistor, a collector of the PNP transistor is connected to a base of the NPN transistor and further through a resistor ~~R_N~~ (R_N) to a ground terminal, where the base of the PNP transistor serves as a gate of the SCS;

a switch control circuit connected between the negative power supply node and the gate of the SCS;

a metal oxide semiconductor field effect transistor (MOSFET) having a drain, ~~and~~ a source and a gate, ~~which~~ wherein the drain and the source of the MOSFET are respectively connected to the SCS and the ground terminal, and the gate of the MOSFET is ~~having a gate~~ coupled to a transistor control circuit wherein the MOSFET can cause the SCS to be triggered into a conduction status~~,~~; and

the transistor control circuit ~~being~~ is connected between the positive power supply node and the MOSFET;

~~such that~~ whereby when forward over-voltage stress occurs over the positive power

supply node, ~~enables~~ the transistor control circuit is enabled to turn on the MOSFET, and at the same time the switch control circuit is enabled to trigger the SCS into a conduction status to form a discharging path, ~~thereby to decrease~~ such that a terminal voltage over the positive power supply node is decreased to a level of a holding voltage of the SCS to provide an ESD protection and prevent latch-up of the SCS.